IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
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STATEMENT UNDER 37 C.F.R. 3.73(b)

Pursuant to 37 C.F.R. 3.73(b), Analog Devices, Inc., a Massachusetts corporation having its principal place of business at One Technology Way, P. O. Box 9106, Norwood, MA 02062-9106 (hereinafter "Assignee") hereby states that it is the assignee of entire right, title, and interest in each of the following patents and patent applications, through the following assignments recorded with the U.S. Patent and Trademark Office and/or enclosed herewith:

Atty. Docket	Application No.	Filing Date	Title	Inventor(s)	Reel	Frame
ANA-087	11/224495	9/12/2005	Digital Signal Processor Optimized for Interpolation and Decimation	DOMINGO	ATTACHED	
ANA-088	10/786,250	2/25/2004	Cache Memory with Improved Replacement Policy	SCHUBERT	015480	0540
ANA-089	10/951,319	9/27/2004	Improvements in Multicarrier Modulation Systems	ARMSTRONG and BREWER	016129	0802
ANA-090	11/704,143	2/8/2007	Metrics Modules and Methods for Monitoring, Analyzing and Optimizing Bus and Memory Operations in a Complex Integrated Circuit	SYED, GENTILE and KOKER	019250	0865
ANA-091	11/157,650	6/21/2005	Methods and Apparatus for an Efficient Floating Point ALU	SRIVASTAVA	016715	0044
ANA-093	11/209,477	8/23/2005	System and Method for Automated Verification of Performance and Budget Goals in a Process	KAFKA, ARONOV, and GOVONI	016917	0365
ANA-094	11/890,907	8/8/2007	Implementation of Variable Length Instruction Encoding Using Alias Addressing	GIRI and NADIG	020123	0888
ANA-095	12/217,563	1/7/2008	Methods and Apparatus for Predictable Level Shifter Power-Up State	FOLEY and LI	021622	0609
ANA-097	12/412974	3/27/2009	Method and Apparatus for Scaling Signals to Prevent Amplitude Clipping	CHALIL	022778	0135

Atty. Docket	Application No.	Filing Date	Title	Inventor(s)	Reel	Frame
ANA-098	12/136,492	6/10/2008	Half Pixel Interpolator for Video Motion Estimation Accelerator	COX, BOTCHEV, NING, ZHANG, and HOFFMAN	021101	0644
ANA-099A	11/818,449	6/14/2007	Software Programmable Timing Architecture	OLOFSSON, JACOBS, and KETTLE	019876	0255
ANA-099B	11/818,452	6/14/2007	Software Programmable Timing Architecture	OLOFSSON	019876	0271
ANA-099C	11/998,994	12/3/2007	A Variable Instruction Width Software Programmable Data Pattern Generator	OLOFSSON, JACOBS, and KETTLE	020873	0549
ANA-100	12/070,224	2/15/2008	Output Driver with Overvoltage Protection	BOYKO and PATTERSON	020567	0221
ANA-101	11/623,760	1/17/2007	Novel Context Instruction Cache Architecture for a Digital Signal Processor	RINGE and GIRI	018762	0929
ANA-102	11/304,294	12/15/2005	Method for Locking a Synthesised Output Signal of a Synthesised Waveform Synthesiser in a Phase Relationship with an Input Signal, and a Digital Waveform Synthesiser for Producing a Synthesised Output Signal in a Phase Relationship with an Input Signal	TUCHOLSKI	017550	0633
ANA-102C1	12/546,738	8/25/2009	Method for Locking a Synthesised Output Signal of a Synthesised Waveform Synthesiser in a Phase Relationship	TUCHOLSKI	017550	0633
ANA-104C1	11/637,232	12/11/2006	Cache Memory Background Preprocessing	GREENFIELD and SALITERNIK	015020	0442
ANA-105	11/584,147	10/20/2006	File Attributes for Flexible Linking	KILBANE and RAIKMAN	018712	0303
ANA-106	11/584,183	10/20/2006	Process for Handling Shared References to Private Data	KILBANE and RAIKMAN	018712	0299
ANA-107	11/821,847	6/26/2007	Methods and Apparatus for Automation of Register Maps	DHARMAGADDA	019663	0698
ANA-108	12/008,335	1/10/2008	Multi-Format Multiplier Unit	OLOFSSON and YANOVITCH	020691	0440

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ANA-109D1	12/470813	5/22/2009	Integrated Circuits with Programmable Well Biasing	OLOFSSON	020378	0921
ANA-110	10/992,939	11/19/2004	System and Method for Sub-Pixel Interpolation in Motion Vector Estimation	NAGARAJAN	016022	0283
ANA-111	12/008,334	1/10/2008	Bandwidth Efficient Instruction-Driven Multiplication Engine	OLOFSSON and YANOVITCH	021009	0075
ANA-113	11/643,445	12/1/2006	Method and Apparatus for Progressive Scanning of Interlaced Video	PAN and LIS	018975	0877
ANA-120	09/923,225	8/6/2001	High Performance Turbo and Viterbi Channel Decoding in Digital Signal Processors	PLANTE and GREENFIELD	012518	0649
ANA-121	12/365,386	2/4/2009	Method and Apparatus for Hardware Reset Protection	GIORDANO and BIEDERWOLF	022558	0566
ANA-122	12/328,464	12/4/2008	Method and Apparatus for Performing Jump Operations in a Digital Processor	MAYER, BAHADOOR and LONG	022265	0560
ANA-123	11/152,875	6/15/2005	Method and Apparatus for Deep Sub-Micron Design of Integrated Circuits	RAMAKRISHNAN and PADMANABHAN	016694	0835
ANA-124	12/362,994	1/30/2009	Method and Apparatus or Software GPS Receiver	AN and STEIN	022534	0302
ANA-125	11/638,951	12/14/2006	Randomly Sub-Sampled Partition Voting (RSPB) Algorithm for Scene Change Detection	HOFFMAN, ZHANG, and NING	018944	0186
ANA-126	11/638,838	12/14/2006	Motion Estimation Using Prediction Guided Decimated Search	HOFFMAN, ZHANG, SINGH, and NING	019118	0365
ANA-127	12/008,220	1/9/2008	Processor Architectures for Enhanced Computational Capability	GARDE	020389	0487
ANA-128	11/488,484	7/18/2006	Automatic Environmental Compensation of Capacitance Based Proximity Sensors	FEEN, COQUEREL, JEYAPAUL, and CLEARY	018113	0881
ANA-133	11/531,698	9/14/2006	A Technique to Visually Present Memory Location and Usage during Code Execution	ANDERSON	018349	0149

Atty. Docket	Application No.	Filing Date	Title	Inventor(s)	Reel	Frame
ANA-135	11/566,692	12/5/2006	System and Method for an Efficient Comparison Operation of Multi-Bit Vectors in a Digital Logic Circuit	GIRI	018581	0481
ANA-140D1	12/463,612	5/11/2009	DMA Controller for Digital Signal Processors	HAYDEN	015673	0199
ANA-141	12/365,251	2/4/2009	J-TAG Emulation Control during Protected Modes of Operation within LockboxTM	GIORDANO and BIEDERWOLF	022558	0610
ANA-142	12/070,280	2/15/2008	Differential Current Output Driver with Overvoltage Protection	BOYKO and CHE	020574	0400
ANA-143A	12/269,615	11/12/2008	Methods and Apparatus for Generating and Processing Transmitter Signals	DELIWALA	022211	0871
ANA-143B	12/269,646	11/12/2008	Methods and Apparatus for Generating and Processing Transmitter Signals	DELIWALA	022210	0738
ANA-144	12/188,634	8/8/2008	Compute Block for Efficient FFT and FIR Hardware Acceleration	LERNER	021464	0011

As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

The undersigned, whose title is supplied below, is authorized to act on behalf of the Assignee.

Respectfully submitted,

Dated: 11-2-09

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